Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of performing time drift compensation in a receiver, the method comprising the steps of:

receiving a signal, which comprises chips, at the receiver;

producing a control pulse after having received a certain number of chips of the received signal;

controlling a variable delay applied to the received signal;

sending, to demodulation units in the receiver, a delayed signal in which chips have been omitted or duplicated on the basis of said control pulse;

supplying, to said demodulation units in the receiver, a compensation signal that indicates whether chips have been omitted or duplicated in the delayed signal; and

demodulating the delayed signal such that the demodulation units consider the omission or duplication of chips in the delayed signal.

2. (Currently Amended) The method according to claim 1, further comprising the step of synchronizing the compensation signal to the control pulse.

3. (Previously Presented) The method according to claim 1, further comprising the step of aligning said control pulse with a symbol boundary.

4. (Previously Presented) The method according to claim 1, wherein the received signal comprises both data chips and pilot chips and the step of demodulating is performed in a first and a second demodulation unit and further comprises the step of:

demodulating the received pilot chips in the first demodulation unit to produce demodulated pilot chips and the received data chips in the second demodulation unit to produce demodulated data chips.

5. (Previously Presented) The method according to claim 1, wherein the compensation signal is given a first value which indicates that a chip has been omitted in the delayed signal and a second value which indicates that a chip has been duplicated in the delayed signal.

6. (Previously Presented) The method according to claim 1, wherein the step of demodulating chips comprises the steps of:

descrambling the delayed chips; and

despreading the descrambled chips.

7. (Currently Amended) The method according to claim 4, further comprising the step of:

integrating the demodulated pilot chips to create a pilot symbol and the demodulated data chips to create a data symbol[[;]].

8. (Previously Presented) The method according to claim 7, wherein said first and second values of the compensation signal control scrambling codes and spreading codes sent to the demodulation units such that a chip is omitted in the respective code on reception of a compensation signal having a first value, and a

chip is duplicated in the respective code on reception of a compensation signal having a second value, and wherein said first and second value of the compensation signal further control the integrators such that a chip is omitted in the integration on reception of the first value, and a chip is duplicated in the integration on reception of the second value.

9. (Previously Presented) The method according to claim 8, further comprising the steps of:

delivering, from the first demodulation unit to the second demodulation unit channel estimation information derived from the pilot symbol; and

employing said channel estimation information at the second demodulation unit to improve said data symbol by taking into account channel parameters.

10. (Currently Amended) A receiver for performing time drift compensation, the receiver comprising:

a timer;

a common delay unit; and

demodulation units[[;]], wherein the timer is arranged to produce a control pulse after having received a certain number of chips of a received signal;

the common delay unit is arranged to apply a variable delay to the received signal and thus send a delayed signal to the demodulation units in the receiver, in which delayed signal chips have been omitted or duplicated on the basis of said control pulse;

the timer is further arranged to supply, to said demodulation units in the receiver, a compensation signal that indicates whether chips have been omitted or duplicated in the delayed signal; and

the demodulation units are arranged to demodulate the delayed signal such that the demodulation units consider the omission or duplication of chips in the delayed signal.

11. (Previously Presented) The receiver according to claim 10, wherein the timer is further arranged to synchronize the compensation signal to the control pulse.

12. (Previously Presented) The receiver according to claim 10, wherein the timer is further arranged to align said control pulse with a symbol boundary.

13. (Previously Presented) The receiver according to claim 10, wherein the received signal comprises both data chips and pilot chips and the demodulation is performed in a first and a second demodulation unit, the first demodulation unit being further arranged to demodulate the received pilot chips to produce demodulated pilot chips and the second demodulation unit being further arranged to demodulate the received data chips to produce demodulated data chips.

14. (Previously Presented) The receiver according to claim 10, wherein the timer is further arranged to give the compensation signal a first value which indicates that a chip has been omitted from the delayed signal and a second value which indicates that a chip has been duplicated in the delayed signal.

15. (Previously Presented) The receiver according to claim 10, wherein the demodulation units comprises:

descrambling code generators employed to descramble the delayed chips; and

despreading code generators employed to despread the descrambled chips.

16. (Previously Presented) The receiver according to claim 10, wherein the demodulation units comprises:

integrators arranged to integrate the demodulated pilot chips to create a pilot symbol and the demodulated data chips to create a data symbol.

17. (Previously Presented) The receiver according to claim 10, wherein said first and second values of the compensation signal control scrambling codes and spreading codes supplied to the demodulation units such that a chip is omitted from the respective code on reception of a compensation signal having a first value, and a chip is duplicated in the respective code on reception of a compensation signal having a second value, and wherein said first and second value of the compensation signals further control the integrators such that a chip is omitted in the integration on reception of the first value, and a chip is duplicated in the integration on reception of the second value.

18. (Previously Presented) The receiver according to claim 17, further comprising:

a channel estimation integrator arranged to deliver, from the first demodulation unit to the second demodulation unit channel estimation information derived from the pilot symbol, wherein said channel estimation information is employed at the second demodulation unit to improve said data symbol by taking into account channel parameters.

19. (New) A receiver for performing time drift compensation, the receiver comprising:

a timer;

a common delay unit; and

demodulation units,

wherein the timer is arranged to produce a control pulse after having received a certain number of chips of a received signal,

wherein the common delay unit is arranged to apply a variable delay to the received signal and thus send a delayed signal to the demodulation units in the receiver, in which delayed signal chips have been omitted or duplicated on the basis of said control pulse,

wherein the timer is arranged to supply, to said demodulation units in the receiver, a compensation signal that indicates whether chips have been omitted or duplicated in the delayed signal,

wherein the demodulation units are arranged to demodulate the delayed signal such that the demodulation units consider the omission or duplication of chips in the delayed signal, and

wherein the received signal comprises both data chips and pilot chips and the demodulation is performed in a first and a second demodulation unit, the first demodulation unit being further arranged to demodulate the received pilot chips to produce demodulated pilot chips and the second demodulation unit being further arranged to demodulate the received data chips to produce demodulated data chips.

20. (New) The receiver according to claim 19, wherein said first and second values of the compensation signal control scrambling codes and spreading codes supplied to the demodulation units such that a chip is omitted from the respective

code on reception of a compensation signal having a first value, and a chip is duplicated in the respective code on reception of a compensation signal having a second value, and wherein said first and second value of the compensation signals further control the integrators such that a chip is omitted in the integration on reception of the first value, and a chip is duplicated in the integration on reception of the second value.

21. (New) The receiver according to claim 19, further comprising:

a channel estimation integrator arranged to deliver, from the first demodulation unit to the second demodulation unit, channel estimation information derived from the pilot symbol, wherein said channel estimation information is employed at the second demodulation unit to improve said data symbol by taking into account channel parameters.